the Drawings for lack of a proper legend in Figures 1 and 2.

The applicant has amended Figures 1 and 2 to include a legend "Prior Art", and thus believes the formality deficiency has been overcome.

The applicant respectfully traverses the rejections of the Examiner on the pending claims 1-20, as explained in detail below.

The present invention teaches a novel circuit for input side impedance matching of a power amplifier, which comprises an impedance transformer network to synthesize the predetermined impedance of the source signal at the input of the power amplifier. In particular, as taught by the present invention, the impedance transformer network, which is to synthesize the predetermined impedance at the input of the power amplifier, is joined in parallel with the source and comprises a negative resistor in series with an inductor, as explicitly defined in independent claims 1, 10 and 15. The novel arrangement of the present invention solves the problems of reduced signal swing existing in the prior art where a LC matching circuit is utilized as the impedance transformer network to synthesize the predetermined impedance at the input of the amplifier.

The applicant does not agree with the assertion of the Examiner that the present invention as defined in independent claim 1 has been anticipated in Utsu et al (US Patent No. 5,343,172). In particular, the applicant does not agree with the Examiner that the parallel variable reactance circuit 14 be read as the impedance transformer network of the present invention as claimed.

As expressly defined in claim 1, the impedance transformer network is a network to synthesize the predetermined impedance of the source signal at the input of the power amplifier, while the parallel variable reactance circuit 14 in Utsu patent does NOT synthesize the predetermined impedance at the input of the amplifier (FET 11). As clearly described and illustrated throughout Utsu patent, the circuit 14 is only a part of the matching circuit which further includes a series reactance 12, 31 or 44. For example, it is clearly described in Utsu that "the matching circuit is thus

constituted by the reactance circuits 12 to 15" (see col. 3, lines 53-54) and that "an input matching circuit constituted by a series reactance 44 and a parallel variable reactance circuit 45..." (see col. 5, lines 13-15). Thus, it is the whole matching circuit which includes both the parallel variable reactance circuit 14 and the series reactance 12, 31 or 44, but not the parallel variable reactance circuit 14, that synthesizes the predetermined impedance at the input of amplifier (FET 11). Therefore, the whole matching circuit, but not the parallel variable reactance circuit 14, should be read as the impedance transformer network in claim 1 which is defined as to synthesize the predetermined impedance at the input of amplifier. As can be seen clearly in Figures 1, 3 and 4, the parallel reactance circuit 14 does not directly connect to the input of FET 11 but through the series reactance 12, 31 or 44, thus the circuit 14 does not synthesize an impedance at the input of amplifier (FET 11), but only at the point where it is connected to the reactance 12, 31 or 44. In other words, the parallel variable reactance circuit 14 does NOT synthesize the predetermined impedance at the input of the amplifier, and therefore is not proper to be read as the impedance transformer network defined in claim 1.

Furthermore, the applicant does not agree with the assertion of the Examiner that the reactance 12, 31 or 44 of the matching circuit in the Utsu patent is not an important part of the whole matching circuit. No support for such an assertion can be found in Utsu patent, and the importance of the variable parallel reactance circuit 14 in Utsu does not in any way mean that the series reactance can be omitted from the LC matching circuits. To the contrary, it is clearly described and illustrated throughout Utsu patent that the system comprises the series reactance (see Figures 1, 3 and 4, and col. 3, lines 53-54, col. 4, lines 57-63 and col. 5, lines 13-16). In fact, Utsu is an improvement on its prior art shown in Figures 6A and 6B which utilizes two typical LC matching circuits, each comprising a parallel reactance and a series reactance. In particular, Utsu teaches a novel arrangement in the parallel reactance part of the LC matching circuit, whereby "when a variable reactance circuit 32 is set and parallelly combined with a series reactance 31, a variable matching circuit having a very low loss

can be constituted like a matching micro-strip reactance circuit shown in Fig. 6B which is constituted by strip lines 62, 63, 64, and 65", and "the monolithic MIC amplifying circuit ... can obtain almost the same performance as that of the ideally designed circuit shown in Fig. 6A" (see col. 4, line 58 – col. 5, line 1).

Summing up the above, the applicant believes that it is the whole variable matching circuit but not the variable parallel reactance circuit 14 that must be read as the impedance transformer network in claim 1. As clearly shown in Figures 1, 3 and 4, with the series reactance 12, 31 and 44, the matching circuit in the Utsu patent is NOT in parallel with the source, as defined in independent claim 1.

Therefore, the applicant believes that independent claim 1, with the distinguishing features that the impedance transformer network to synthesize the predetermined impedance at the input of the power amplifier is in parallel with the source, is not anticipated by Utsu patent under 35USC 102(b), and is thus patentable.

The above distinguishing features can not be found in Lleveland et al (WO 98/47190) either, and therefore independent claims 10 and 15, both including the above distinguishing features, can not be reached from a combination of the Utsu and Lleveland, and are thus also patentable for the same explanation as to claim 1.

At least for the same reasons, the applicant believes dependent claims 2-9, 11-14 and 16-20 are also patentable, since each of them includes all the limitations of one of the dependent claims 1, 10 and 15.

The applicant therefore respectfully requests reconsideration and allowance in view of the

above remarks. The Examiner is authorized to deduct additional fees believed due from our Deposit Account No. 11-0223.

Respectfully submitted,

KAPLAN & GILMAN, L.L.P.
900 Route 9 North
Woodbridge, New Jersey 07095
Telephone (732) 634-7634

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Jeffrey I. Kaplan
(Reg. No. 34,356)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Box Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231 on April 4, 2003.

Dated April 4, 2003 Signed _____ Print Name Jeffrey I. Kaplan

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